REMARKS

By this Amendment, Applicants have canceled claim 5 and amended claim. Claims 1-4 and 6-17 are pending in the application. Claims 14-17 have been withdrawn. In view of the amendments and remarks contained herein, favorable reconsideration in this application is respectfully requested.

The Examiner rejected claims 1-13 under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of U.S. Patent No. 6,320,213 to Kirlin et al. ("Kirlin") and U.S. Publication No. 2001/0043453 to Narwankar et al. ("Narwankar").

As set forth in amended claim 1, the present invention is directed to a method for manufacturing a semiconductor device, comprising the steps of providing a semiconductor substrate, forming an interlayer insulating layer on the semiconductor substrate, forming a contact hole in the interlayer insulating layer, forming a plug recessed inside the contact hole, forming an ohmic contact layer on the plug, depositing a layer selected from the group consisting of an La layer and a LaN layer on the ohmic contact layer, performing a nitridation process by a plasma treatment process to form a LaN diffusion barrier layer on the ohmic contact layer, and sequentially forming a bottom electrode, a BLT ($(Bi_xLa_y)Ti_3O_{12}$) dielectric layer and a top electrode on the entire structure, wherein, in the BLT dielectric layer, the atomic concentration of Bi is 3.25 to 3.35 and the atomic concentration of La is 0.80 to 0.90. This is not shown or suggested by the prior art.

The present invention provides the La or the LaN diffusion barrier formed

between the ohmic contact layer and the bottom electrode in the BLT capacitor structure. Since La, which is contained in the BLT layer, is used as the diffusion barrier in the BLT capacitor, when the La is diffused to the BLT layer during a post thermal process, a ferroelectric characteristic of the BLT layer is not degraded.

However, the cited references do not teach or even suggest that the La diffusion barrier, which is formed between the ohmic contact layer and the bottom electrode in the contact hole, is applied in the BLT capacitor structure. Even though the La is contained in PLZT {(Pb, La)(Zr, Ti)O_3} mentioned in the art cited against the present invention, since PLZT has much worse fatigue characteristics than that of the BLT, the improvement to be obtained by using La diffusion barrier layer cannot be expected, representing an unexpected result that is patentable over the prior art.

For at least the foregoing reasons, claim 1 is patentable over the prior art. Claims 2-4 and 6-13 are also in condition for allowance as claims that are properly dependent on an allowable base claim and for the subject matter contained therein. Favorable reconsideration and allowance of the pending claims is requested.

With the foregoing amendments and remarks, the application is in condition for allowance. Should the Examiner have any questions or comments, the Examiner is cordially invited to telephone the undersigned attorney so that the present application can receive an early Notice of Allowance.

Respectfully submitted,

JACOBSON HOLMAN PLLC

By Yoon S Ham by Sage C Bailey
Yoon S. Ham
Reg. No. 45,307
Reg No. 40,425

400 Seventh Street, N.W.
Washington, D.C. 20004
Telephone: (202) 638-6666
Atty Docket: P67350US0
Date: September 22, 2003
YSH:SCB

R:\SBailey\9-03\P67350US.AMD